

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A buck converter comprising:

[[-]] a pair of input terminals A and B for connecting an input DC voltage V_{in} across these two terminals, the potential of the terminal A being higher than the potential of the terminal B;

[[-]] a pair P_0 of switches SB, SH in series and connected to the input terminal B by the switch SB, each switch SB, SH comprising a control input so that, simultaneously, one is set in a conducting state by the application of a first control signal at its control input, and the other in an isolating state by the application of a second control signal, complementary to the first control signal, at its control input;

[[-]] a pair of output terminals C and D for supplying a load R_{out} with an output voltage V_{out} , the output terminal D being connected to the input terminal B and the output terminal C to the connection point between the two switches SB and SH in series via a filter inductor L_{out} , characterized in that it comprises:

[[-]] ~~K other additional pairs $P_1, P_2, \dots, P_i, \dots, P_{K-1}, P_K$ of switches in series between the input terminal A and the switch SH of the pair P_0 , with $i = 1, 2, \dots, K-1, K$, the two switches of the same additional pair P_i being connected in series via an energy recovery inductor L_{r_i} ;~~

[[-]] ~~K input groups, $G_{in_1}, G_{in_2}, \dots, G_{in_i}, \dots, G_{in_{K-1}}, G_{in_K}$, of N_i capacitors C in series, each of the same value,~~

with $i = 1, 2, \dots, K-1, K$ and $N_i = (K+1) - i$, the electrode of the capacitors of one of the two ends of each input group ~~$G_{in_1}, G_{in_2}, \dots, G_{in_i}, \dots, G_{in_K-1}, G_{in_K}$~~ being connected to the input terminal A, at least the electrode of the capacitors of each of the other ends of the input groups ~~$G_{in_1}, G_{in_2}, \dots, G_{in_i}, \dots, G_{in_K-1}, G_{in_K}$~~ being connected to the connection point between two pairs of consecutive switches $P_{(i-1)}$ and P_i , respectively;

[[-]] K output groups, $G_{out_1}, G_{out_2}, \dots, G_{out_i}, \dots, G_{out_K-1}, G_{out_K}$, of M_i capacitors C in series, each of the same value, with $i = 1, 2, K$ and $M_i = i$, the electrode of the capacitors of one of the two ends of each output group $G_{out_1}, G_{out_2}, \dots, G_{out_i}, \dots, G_{out_K-1}, G_{out_K}$ being connected to the common point between the two switches of the pair P_0 , at least the electrode of the capacitors of each of the other ends of the output groups $G_{out_1}, G_{out_2}, \dots, G_{out_i}, \dots, G_{out_K}$ being connected to the common point between each switch SH_i and the recovery inductor Lr_i of the corresponding pair P_i of the same rank i , respectively,

in that the switches of these other K additional pairs are simultaneously controlled by the first and second complementary control signals forming, when the switch SB of the pair P_0 connected to the terminal B is set in the conducting state for a time T_{off} , a first network of capacitors connected between the terminal A and the terminal B, comprising the groups of input capacitors in series with the groups of output capacitors such that a group of input capacitors G_{in_i} is in series, via its respective energy recovery inductor Lr_i , with its respective group of output capacitors G_{out_i} ,

and in that, when the switch SB of the pair P_0 connected to the input terminal B is set in the isolating state, SH being

set in the conducting state, for a time T_{on} , these other K pairs of switches form a second network of capacitors, connected between the terminal A and the output filter inductor L_{out} , comprising the input group G_{in_1} in parallel with the output group G_{out_K} , in parallel with input capacitor groups in series with output capacitor groups such that an input capacitor group G_{in_i} is in series with an output capacitor group G_{out_i} .

2. (currently amended): The buck converter as claimed in claim 1, ~~characterized in that~~ wherein each additional pair P_i of the converter comprises, in parallel, a diode Sc_i in series with an impedance Z_i , the anode of the diode Sc_i being connected to the connection point between the pair P_i and the lower pair P_{i-1} , the common point between the cathode of the diode Sc_i and the impedance Z_i being connected to the common point between the switch SB_i and the recovery inductor Lr_i .

3. (currently amended): The buck converter as claimed in claim 2, ~~characterized in that~~ wherein the impedance Z_i comprises a diode Dd in series with a resistor r , the anode of the diode Dd being connected, in the converter circuit, to the cathode of the diode Sc_i .

4. (currently amended): The buck converter as claimed in claim 2, ~~characterized in that~~ wherein the impedance Z_i comprises the diode Dd in series with a zener diode Dz , the two cathodes of the diode Dd and the zener diode Dz being connected together, the anode of the diode Dd being connected, in the converter circuit, to the cathode of the diode Sc_i .

5. (currently amended): The buck converter as claimed in ~~one of claim[s]] 1 to 4,~~ wherein it does not comprise interconnections between the capacitors of the same potential level, each of the input groups G_{in_i} or output groups

Gout_i respectively comprising a single capacitance Cea₁, Cea₂;...Cea_i...Ce_K for the input group Gin_i and Csa₁, Csa₂;... Csa_i... Csa_K for the output groups Gout_i, and in that the value of each of these input capacitances Ce_i can be deduced by the calculation of the resultant capacitance of

Ni = (K+1)-i capacitors C in series, with i = 1, 2,...K, i being the order of the input group in question:

$$\begin{aligned} \text{Cea}_1 &= C/K & i &= 1 \\ \text{Cea}_2 &= C/(K-1) & i &= 2 \\ &\dots & & \\ \text{Cea}_i &= C/((K+1)-i) & i & \\ &\dots & & \\ \text{Cea}_K &= C & i &= K \end{aligned}$$

in that value of each of these output capacitances Csa_i can be deduced by the calculation of the resultant capacitance of Mi = i capacitors C in series, i being the order of the output group in question:

$$\begin{aligned} \text{Csa}_1 &= C & i &= 1 \\ \text{Csa}_2 &= C/2 & i &= 2 \\ &\dots & & \\ \text{Csa}_i &= C/i & i & \\ &\dots & & \\ \text{Csa}_K &= C/K & i &= K \end{aligned}$$

6. (currently amended): The buck converter as claimed in ~~one of claim[[s]] 1 to 4, characterized in that~~ wherein it comprises interconnections between the capacitors of the same potential level Nv, the structure comprising a single input

group G_{in} and a single output group G_{out} , the input capacitance of each of the potential levels N_{in_i} , i being the order of the potential level in question at the input, in parallel with its respective pair P_i , is deduced by calculating the capacitance C_{eb_i} equivalent to the capacitors in parallel of the level N_{in_i} in question, which is:

$$\begin{aligned} C_{eb_1} &= C.K & i &= 1 \\ C_{eb_2} &= C.(K-1) & i &= 2 \\ &\dots\dots\dots \\ C_{eb_i} &= C.((K+1)-i) & i & \\ &\dots\dots\dots \\ C_{eb_K} &= C & i &= K \end{aligned}$$

in that the output capacitance of each of the potential levels N_{out_i} , in parallel between two consecutive pairs pair P_i , P_{i-1} , is deduced by calculating the capacitance C_{sb_i} equivalent to the capacitors in parallel of the level N_{out_i} in question, i being the order of the output potential level in question, which is:

$$\begin{aligned} C_{sb_1} &= C.K & i &= 1 \\ C_{sb_2} &= C.(K-1) & i &= 2 \\ &\dots\dots\dots \\ C_{sb_i} &= C.((K+1)-i) & i & \\ &\dots\dots\dots \\ C_{sb_K} &= C & i &= K \end{aligned}$$

7. (currently amended): The buck converter as claimed in ~~one of claim[[s]] 1 to 4, characterized in that~~ wherein it comprises combinations of capacitors in parallel for certain groups and in series for others.

8. (currently amended): The buck converter as claimed in ~~one of claim[[s]] 1 to 7, characterized in that~~ wherein it comprises K recovery transformers, the primary of a transformer of order Tr_i being connected between the two switches of the additional pair P_i , the secondary being connected, at one end, to the terminals B and D of the converter and, at the other end, to the input terminal A via a zener diode Zb_i whose cathode is connected to said input terminal A.

9. (currently amended): The buck converter as claimed in ~~one of claim[[s]] 1 to 7, characterized in that~~ wherein it comprises K recovery transformers, the primary of a transformer of order Tr_i being connected between the two switches of the additional pair P_i , the secondary being connected, at one end, to the terminals B and D of the converter and, at the other end, to the output resistance R_{out} via a zener diode Zb_i whose cathode is connected to said output resistance, the transfer of energy stored in the inductor occurring toward the output load R_{out} .

10. (currently amended): The buck converter as claimed in ~~one of claim[[s]] 1 to 9, characterized in that~~ wherein it comprises a current return diode D across the terminals of the switch SB whose anode is connected on the side of the terminals B and D, and an output filter capacitor C_{out} in parallel with the load R_{out} between the output terminals C and D.

11. (currently amended): The buck converter as claimed in ~~one of claim[[s]] 1 to 10, characterized in that~~ wherein the

'flywheel' diodes Sc_1, \dots, Sc_i , the diode D ensuring the current continuity in the output inductor L_{out} and the diodes D_d of the impedance Z_i are silicon diodes.

12. (currently amended): The buck converter as claimed in ~~one of claim[[s]] 1 to 9, characterized in that~~ wherein the 'flywheel' diodes Sc_1, \dots, Sc_i , the diode D ensuring the current continuity in the output inductor L_{out} and the diodes D_d of the impedance Z_i are Schottky diodes.

13. (new): The buck converter as claimed in claim 2, wherein it does not comprise interconnections between the capacitors of the same potential level, each of the input groups G_{in_i} or output groups G_{out_i} respectively comprising a single capacitance $C_{ea_1}, C_{ea_2}; \dots, C_{ea_i} \dots C_{e_K}$ for the input group G_{in_i} and $C_{sa_1}, C_{sa_2}; \dots, C_{sa_i} \dots C_{sa_K}$ for the output groups G_{out_i} , and in that the value of each of these input capacitances C_{e_i} can be deduced by the calculation of the resultant capacitance of

$N_i = (K+1)-i$ capacitors C in series, with $i = 1, 2, \dots, K$, i being the order of the input group in question:

$$C_{ea_1} = C/K \quad i = 1$$

$$C_{ea_2} = C/(K-1) \quad i = 2$$

....

$$C_{ea_i} = C/((K+1)-i) \quad i$$

.....

$$C_{ea_K} = C \quad i = K$$

in that value of each of these output capacitances C_{sa_i} can be deduced by the calculation of the resultant capacitance

of $M_i = i$ capacitors C in series, i being the order of the output group in question:

$$\begin{array}{ll} C_{sa_1} = C & i = 1 \\ C_{sa_2} = C/2 & i = 2 \\ \dots & \\ C_{sa_i} = C/i & i \\ \dots & \\ C_{sa_K} = C/K & i = K \end{array}$$

14. (new): The buck converter as claimed in claim 2, wherein it comprises interconnections between the capacitors of the same potential level N_v , the structure comprising a single input group G_{in} and a single output group G_{out} , the input capacitance of each of the potential levels N_{in_i} , i being the order of the potential level in question at the input, in parallel with its respective pair P_i , is deduced by calculating the capacitance C_{eb_i} equivalent to the capacitors in parallel of the level N_{in_i} in question, which is:

$$\begin{array}{ll} C_{eb_1} = C.K & i = 1 \\ C_{eb_2} = C.(K-1) & i = 2 \\ \dots & \\ C_{eb_i} = C.((K+1)-i) & i \\ \dots & \\ C_{eb_K} = C & i = K \end{array}$$

in that the output capacitance of each of the potential levels N_{out_i} , in parallel between two consecutive pairs pair

P_i , P_{i-1} , is deduced by calculating the capacitance C_{sb_i} equivalent to the capacitors in parallel of the level N_{out_i} in question, i being the order of the output potential level in question, which is:

$$\begin{aligned} C_{sb_1} &= C.K & i &= 1 \\ C_{sb_2} &= C.(K-1) & i &= 2 \\ &\dots\dots\dots \\ C_{sb_i} &= C.((K+1)-i) & i & \\ &\dots\dots\dots \\ C_{sb_K} &= C & i &= K \end{aligned}$$

15. (new): The buck converter as claimed in claim 2, wherein it comprises interconnections between the capacitors of the same potential level N_v , the structure comprising a single input group G_{in} and a single output group G_{out} , the input capacitance of each of the potential levels N_{in_i} , i being the order of the potential level in question at the input, in parallel with its respective pair P_i , is deduced by calculating the capacitance C_{eb_i} equivalent to the capacitors in parallel of the level N_{in_i} in question, which is:

$$\begin{aligned} C_{eb_1} &= C.K & i &= 1 \\ C_{eb_2} &= C.(K-1) & i &= 2 \\ &\dots\dots\dots \\ C_{eb_i} &= C.((K+1)-i) & i & \\ &\dots\dots\dots \\ C_{eb_K} &= C & i &= K \end{aligned}$$

in that the output capacitance of each of the potential levels N_{out_i} , in parallel between two consecutive pairs pair P_i , P_{i-1} , is deduced by calculating the capacitance C_{sb_i} equivalent to the capacitors in parallel of the level N_{out_i} in question, i being the order of the output potential level in question, which is:

$$\begin{aligned} C_{sb_1} &= C.K & i &= 1 \\ C_{sb_2} &= C.(K-1) & i &= 2 \\ &\dots & & \\ C_{sb_i} &= C.((K+1)-i) & i & \\ &\dots & & \\ C_{sb_K} &= C & i &= K \end{aligned}$$

16. (new): The buck converter as claimed in claim 2, wherein it comprises K recovery transformers, the primary of a transformer of order Tr_i being connected between the two switches of the additional pair P_i , the secondary being connected, at one end, to the terminals B and D of the converter and, at the other end, to the input terminal A via a zener diode Zb_i whose cathode is connected to said input terminal A.

17. (new): The buck converter as claimed in claim 2, wherein it comprises K recovery transformers, the primary of a transformer of order Tr_i being connected between the two switches of the additional pair P_i , the secondary being connected, at one end, to the terminals B and D of the converter and, at the other end, to the output resistance R_{out} via a zener diode Zb_i whose cathode is connected to said output resistance,

the transfer of energy stored in the inductor occurring toward the output load R_{out} .

18. (new): The buck converter as claimed in claim 2, wherein it comprises a current return diode D across the terminals of the switch SB whose anode is connected on the side of the terminals B and D , and an output filter capacitor C_{out} in parallel with the load R_{out} between the output terminals C and D .

19. (new): The buck converter as claimed in claim 2, wherein the 'flywheel' diodes Sc_1, \dots, Sc_i , the diode D ensuring the current continuity in the output inductor L_{out} and the diodes D_d of the impedance Z_i are silicon diodes.

20. (new): The buck converter as claimed in claim 2, wherein the 'flywheel' diodes Sc_1, \dots, Sc_i , the diode D ensuring the current continuity in the output inductor L_{out} and the diodes D_d of the impedance Z_i are Schottky diodes.